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09/852,735	05/11/2001	Mototsugu Okushima	NE212-US	4991

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YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER
KITOV, ZEEV

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2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/852,735	Applicant(s) OKUSHIMA, MOTOTSUGU	
	Examiner Zeev Kitov	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 36* is/are rejected.

7)☒ Claim(s) *1,2,7 and 9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Objections

1. Claims 1 and 11 are objected due to following statement: "electric charge .... being electrically communicated", which does not make a sense, because a term communication implies transmitting information, which is not the case in the claim. It should be rephrased as, for example, "electric charge .... being conducted" or " being discharged", or "being removed". Additionally, the same statement is recited in an Abstract and numerous times in the Specification. Appropriate corrections are required.

2. Claims 2, 7 and 10 are objected due to following statement: "said breakdown is a substantial breakdown owing to conduction" (emphasis added). A term "substantial breakdown" is not found in technical vocabularies. Specification recites the term without giving its definition. While applicant may be his/her own lexicographer, for introduction of a new term, he/she needs to provide a clear definition of the term. An applicant apparently believes that the term serves a purpose of definite limitation. But it does not, because a technical meaning of the term is not clear. Appropriate correction is required. For purpose of examination, the recited statement was considered as: "said breakdown is due to a forward bias conduction".

3. Claims 9 and 10 are objected to due to a lack of antecedent basis. Recited "said first diode", "said first resistor", "said first longitudinal bipolar transistor" and "said second diode", said second resistor", "said second longitudinal bipolar transistor" have

no antecedent basis neither in instant claims, nor in preceding Claims 1 or 2. Appropriate correction is required.

4. Claims 9 and 10 are further objected to due to a following reason. The mentioned recitations do not make a sense, because neither Claims 9 or 10, nor preceding Claims 1 or 2 recite "first diode", "second diode" e t. c. Therefore, there is no way of making selection to provide only one of two diodes, two resistors or two transistors. Appropriate correction is required.

5. Claim 12 is objected to due to a typographical error. On page 44, lines 22 and 24 the word "pad" is erroneously written in plural form, while there is no antecedent basis for "pads". Appropriate correction is required.

6. Claims 16 – 36 are objected due to a following reason. The claims recite an ESD protection apparatus, which is identified by its schematic structure. Claims 16 – 36 while claiming the apparatus, recite manufacturing process of the apparatus, which according to MPEP definition are product-by-process claims. The process of Claims 16 – 36 does not change the claimed end product, which can be manufactured by variety of ways.

According to MPEP 2113: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted) (Claim was directed to a novolac color developer. The process

of making the developer was allowed. The difference between the inventive process and the prior art was the addition of metal oxide and carboxylic acid as separate ingredients instead of adding the more expensive pre-reacted metal carboxylate. The product-by-process claim was rejected because the end product, in both the prior art and the allowed process, ends up containing metal carboxylate. The fact that the metal carboxylate is not directly added, but is instead produced in-situ does not change the end product).

These claims are in improper dependent form because they fail to further limit the independent claim as required by 37 CFR 1.75(c).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 3, 4, 7, 8, 9, 10, 12, and 14 are rejected under 35 U.S.C. 112 2nd paragraph as being indefinite. A reason for that follows.

A broad range of limitation together with a narrow range of limitation that falls within the broad range of limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the

feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, the listed above claims recite the broad recitation as a circuit comprising two parts with similar structure having two transistors, two diodes and two resistors, and the claims also recite "at least either of said first diode, said first resistor and said first longitudinal bipolar transistor or said second diode, said second resistor and said second longitudinal bipolar transistor are provided", which is the narrower statement of the range/limitation. For purpose of examination the narrower statement of the range/limitation was addressed. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5, 18 – 32 and 34 – 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (US 5,623,387). Li et al. disclose all the elements of the claim, including an ESD protection apparatus installed between a pad of a semiconductor integrated circuit chip element 101 in Fig. 4a) and an inner circuit of the chip (elements T3 and T4 in Fig. 4a) comprising a trigger element having a diode

(element Z124 in Fig. 4a) to be broken down by an over-voltage applied to the pad and a longitudinal bipolar transistor (element T124 in Fig. 4a, col. 8, lines 15 – 67, col. 9, lines 1 - 11) for discharging the electric charge of the pad due to the breakdown of the diode. As to claimed longitudinal structure of the transistor, Li et al. discloses transistor T124 as a lateral transistor (col. 11, lines 28 – 51).

Regarding Claim 3, Li et al. disclose an apparatus having a first and second trigger elements comprising first and second diodes (elements Z124 and Z126 in Fig. 4c) and first and second resistors (elements R124b and R126b in Fig. 4c), NPN type first and second longitudinal transistors (elements T124 and T126 in Fig. 4c), a cathode of the first diode (element Z124 in Fig. 4c) is connected to the input pad and its anode is connected to the base of the first transistor (element T124 in Fig. 4c); a cathode of the second diode is connected to an electric power source (element Z126 in Fig. 4c connected to Vcc) and its anode is connected to the base of the second transistor (element T126 in Fig. 4c); the first resistor (element R124b in Fig. 4c) is connected bet6ween the anode of the first diode and a ground terminal and the second resistor is connected between the anode of the second diode and the pad (see Fig. 4c). A collector of the first longitudinal transistor is connected to the pad and an emitter of the transistor is connected to the ground terminal (see Fig. 4c); the collector of the second transistor is connected to the electric power source terminal and the emitter of the second transistor is connected to the pad (see Fig. 4c). All of the recited elements of the claim are provided.

Regarding Claim 5, Li et al. disclose an apparatus protecting the circuit against ESD discharge through electrical power source terminal, having the longitudinal bipolar NPN transistor (element T121 in Fig. 4c), the cathode of the diode is connected to the power source terminal (Vcc in Fig. 4c) and the anode is connected to the base of the transistor (see Fig. 4c), a resistor is connected between the anode of the diode and a ground terminal (Vss in Fig. 4c) and the collector of the transistor is connected to the power supply pad and the emitter is connected to the ground terminal (Vss in Fig. 4c).

Regarding Claims 18 – 32 and 34 – 36, these claims do not add any identifiable apparatus limitations and therefore are rejected along with the Claim 1, from which they depend. See discussion above regarding MPEP 2113.

3. Claims 11, 13, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Avery (US 5,043,782).

Avery discloses all the elements of Claim11, including a trigger element having a first longitudinal bipolar transistor (element Qs in Fig. 7) whose collector-base junction acts as a diode to be broken by over-voltage applied to the pad (element 20 in Fig. 7) and which discharges the ESD charge of the pad (col. 6, lines 37 – 68, col. 7, lines 1 – 2) and an ESD protection element having a second longitudinal bipolar transistor for discharging the charge of the pad (elements Ql in Fig. 7). According to Avery (col. 4, lines 38 – 42), the pad (element 102 in Fig. 1) may be a voltage supply terminal or an input or output signal terminal.

Regarding Claim 13, Avery discloses the first and second longitudinal bipolar transistors of NPN type (elements Qs and QI in Fig. 7) having their collectors connected to the pad (elements 102 in Fig. 1 and 20 in Fig. 7), which according to Avery (col. 4, lines 38 – 42), may be a power source terminal; the first and second bipolar transistors (elements Qs and QI in Fig. 7) are of NPN type and have their collectors connected to the pad, their bases connected to each other and their emitters connected to the ground terminal (elements 22 in Fig. 1 and 7) and a resistor connected between the bases of transistors and the ground terminal (element Rs in Fig. 7).

Regarding Claims 16 and 17, these claims do not add any identifiable apparatus limitations and therefore are rejected along with the Claim 11, from which they depend. See discussion above regarding MPEP 2113.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 7 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of McClure et al. (US 5,774,318). As was stated above Li et al. disclose all the elements of Claim 1. Regarding Claim 2 they do not disclose the over-voltage as a forward voltage for the diode. McClure et al. disclose the ESD protection circuit wherein the diode is plural diodes (elements 105 in Fig. 2) and the breakdown

(discharge of the ESD charge) occurs due to the diodes conduction. Applying a teaching of McClure et al. to the circuit of Li et al. one of ordinary skill in the art will obtain the Li et al. circuit, wherein two diodes in back biasing direction are replaced by two stack of diodes connected in forward biasing direction. Both patents have the same problem solving area, namely providing efficient ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the McClure et al. solution of forward biased stack of diodes in the circuit of Li et al., because as McClure et al. state (col. 2, lines 45 – 49), it will provide flexible way of setting a breakdown voltage by selecting amount of diodes in the stack.

Regarding Claim 7, Li et al. and McClure et al. disclose all the elements of the claim, including input pad terminal (element 101 in Fig. 4c of Li et al.), two NPN type transistors (elements 106 and 154 in Fig. 3 of McClure), two diodes (elements 115 and 153 in Fig. 3 of McClure) and two resistors (elements R3 and R3' in Fig. 3 of McClure). An anode of the first diode (elements 153 in Fig. 3 of McClure) is connected to the input pad (element 101 in Fig. 4c of Li et al) and a cathode is connected to a base of the first longitudinal bipolar transistor (element 154 in Fig. 3 of McClure); an anode of the second diode (elements 115 in Fig. 3 of McClure) is connected to a power source terminal (elements Vcc in Fig. 4c of Li et al. and Vcc in Fig. 3 of McClure) and its cathode is connected to the base of the second longitudinal bipolar transistor (element 106 in Fig. 3 of McClure); the first resistor (element R3' in Fig. 3 of McClure) is connected between the cathode of the first diode and the ground terminal; the second resistor (element R3 in Fig.3 of McClure) is connected between the cathode of the

second diode and the power supply pad; a collector of the first transistor is connected to the power supply pad and its emitter is connected to the ground terminal; and a collector of the second transistor is connected to the power source terminal and its emitter is connected to the input pad.

Regarding Claim 33, this claim does not add any identifiable apparatus limitations and therefore is rejected along with the Claim 11, from which it depends. See discussion above regarding MPEP 2113.

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of A. Sedra and K. Smith textbook, Microelectronic Circuits. As per Claim 4, it recites a circuit structure of Claim 3, rejected accordingly, wherein PNP transistors replace the NPN transistors and the diodes are connected between the base and collector of the transistor in the same polarity. A. Sedra and K. Smith textbook discloses (Fig. 8.9 and 8.10, pp. 408 – 410) that NPN and PNP transistors are functionally equivalent and differ only in their polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Li et al. circuit (T124 and T126 in Fig. 4c) are subject to this conversion. As per diodes positioning, in Fig. 8.10a the diode equivalent element is a battery Vcb, which according to the mirror conversion rules, it is to be transformed into analog of Vbc battery in Fig. 8.10b having the same polarity, i.e. cathodes of both diodes are to be

connected to the bases of the transistors, while the anode of the first diode is connected to the ground terminal and the anode of the second diode is connected to the pad (power supply terminal). The resistors remain positioned according to Li et al., i.e. between the base and the terminal associated with the emitter. The circuit obtained in such transformation is a full equivalent of the original Li et al. circuit and satisfies all the limitations of Claim 4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Li et al. circuit by replacing NPN transistors by PNP transistors and moving diodes into a new position between the collector and the base accordingly, because as A. Sedra and K. Smith textbook disclose (Fig. 8.9 and 8.10, pp. 408 – 410), NPN and PNP transistors are functionally equivalent and differ only in their polarity. According to them, the schematic solutions with NPN transistors can be converted into solutions with PNP transistors by using mirror reflection polarity change rules. As well known in the art, such conversions are widely used in modern electronic circuit design when for some reasons use of PNP transistors is preferable. Such conversion does not represent a novelty or an inventive step.

As per Claim 6, it recites a circuit structure of Claim 1, rejected accordingly, wherein PNP transistors replace the NPN transistors and the diodes are connected between the base and collector of the transistor in the same polarity. The same mirror replacement as cited above is applicable to the circuit 121 in Fig. 4c of Li et al. Here a longitudinal bipolar transistor (element T121 in Fig. 4c) is connected between the ground and power supply terminals, having a diode connected between its base and

collector, and resistor between its base and emitter. According to A. Sedra and K. Smith textbook (Fig. 8.9 and 8.10, pp. 408 – 410), the NPN transistor circuit can be converted into PNP transistor circuit by mirror placing PNP transistor in reverse polarity and changing place of diode (moving Vcb/Vbc element as in Fig. 8.10a and 8.10b). Replacing T121 transistor in Fig. 4c of Li et al. by PNP transistor according to A. Sedra and K. Smith textbook and placing the diode in the same polarity between the transistor base and the ground terminal results in the PNP transistor circuit fully equivalent to the Li et al. circuit and satisfies all the limitations of Claim 6.

6. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in a view of McClure et al. and further in a view of A. Sedra and K. Smith textbook, Microelectronic Circuits. As was stated above, Li et al. in and McClure et al. disclose all the elements of Claim 2. However regarding Claim 8, they do not disclose the circuit built by using PNP transistors.

A. Sedra and K. Smith textbook discloses (Fig. 8.9 and 8.10, pp. 408 – 410) that NPN and PNP transistors are functionally equivalent and differ only in their polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Li et al. circuit (T124 and T126 in Fig. 4c) are subject to this conversion. As per diodes positioning, in Fig. 8.10a the diode equivalent element is a battery Vcb, which according to the mirror conversion rules, it is

to be transformed into analog of Vbc battery in Fig. 8.10b having the same polarity, i.e. anodes of both diodes are to be connected to the bases of the transistors, while the cathode of the first diode is connected to the ground terminal and the cathode of the second diode is connected to the pad (power supply terminal). The resistors remain positioned according to Li et al., i.e. between the base and the terminal associated with the emitter. The circuit obtained in such transformation is a full equivalent of the original Li et al. circuit and satisfies all the limitations of Claim 8.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Li et al. circuit by replacing NPN transistors by PNP transistors and moving diodes into a new position between the collector and the base accordingly, because as A. Sedra and K. Smith textbook disclose (Fig. 8.9 and 8.10, pp. 408 – 410), NPN and PNP transistors are functionally equivalent and differ only in their polarity. According to them, the schematic solutions with NPN transistors can be converted into solutions with PNP transistors by using mirror reflection polarity change rules. As well known in the art, such modifications are widely used in modern electronic circuit design when for some reasons use of PNP transistors is preferable. Such modification does not represent a novelty or an inventive step.

As per Claim 10, in addition to the limitations of Claim 8 rejected accordingly, it recites the ESD protected pad as being a power supply terminal. McClure et al. disclose the protected pad as the power terminal (element 102 in Fig. 2).

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Avery in a view Li et al.

As was stated above, Avery discloses all the elements of Claim 11. However regarding Claim 12, he does not disclose a dual structure of a protective circuit. Li et al. discloses such a structure having two trigger elements (elements Z124 and Z126 in Fig. 4c), two ESD protection elements (elements T124 and T126 in Fig. 4c) including bipolar NPN transistors and two resistors (elements R124b and R126b in Fig. 4c). When the circuit of Avery is modified according to teaching of Li et al., the obtained circuit will have collectors of bipolar transistors A (element Qs in Fig. 7 of Avery) and C (element QI in Fig. 7 of Avery) connected to the pad (element 20 in Fig. 7 of Avery), their bases are connected to each other and emitters are connected to the ground terminal (element 22 in Fig. 7 of Avery). The first resistor (element Rs is connected between bases of transistors A and C and the ground terminal. At the same according to the teaching of Li et al. the circuit will have a second floor, wherein second pair of transistors, B (element Qs in Fig. 7 of Avery) and D (element QI in Fig. 7 of Avery) have their collectors connected to the power supply terminal (element Vcc in Fig. 4c of Li et al.), their bases are connected to each other and their emitters are connected to the input/output pad (element 101 in Fig. 4c of Li et al.). The second resistor (element Rs in Fig. 7 of Avery) is connected between the bases of transistors B and D and the pad. Both patents have the same problem solving area, namely providing efficient ESD protection for semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the circuit of

Avery using the teaching of Li et al., because as Li et al. state (col. 1, lines 64 – 67, col. 2, lines 1 – 4), an ESD protection circuit should protect the device from an ESD applied between any pair of external pins. These pins include Vcc and ground, as well as input/output.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Avery in a view Li et al. and further in a view of A. Sedra and K. Smith textbook, Microelectronic Circuits. The Claim 14 reciting the limitations of Claim 12, rejected accordingly, additionally requires replacement of NPN transistors by PNP transistors. A. Sedra and K. Smith textbook discloses. A. Sedra and K. Smith textbook discloses (Fig. 8.9 and 8.10, pp. 408 – 410) that NPN and PNP transistors are functionally equivalent and differ only in their polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Avery circuit (Qs and Ql in Fig. 7 of Avery) are subject to this conversion. The resistors remain positioned according to Avery (element Rs in Fig. 7), i.e. between the bases of transistors and the power source terminal (element 20 in Fig. 7 of Avery). According to Li et al. teaching the Avery circuit built with PNP transistors is to be arranged in a two-level structure, similar to Fig. 4c of Li et al. The circuit obtained in such transformation is a full equivalent of the original Avery and Li et al. circuits and satisfies all the limitations of Claim 14.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified combined circuit of Avery and Li et al. by replacing NPN transistors by PNP transistors, because as A. Sedra and K. Smith textbook disclose (Fig. 8.9 and 8.10, pp. 408 – 410), NPN and PNP transistors are functionally equivalent and differ only in their polarity. According to them, the schematic solutions with NPN transistors can be converted into solutions with PNP transistors by using mirror reflection polarity change rules. As well known in the art, such conversions are widely used in modern electronic circuit design when for some reasons use of PNP transistors is preferable. Such conversion does not represent a novelty or an inventive step.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Avery in a view of A. Sedra and K. Smith textbook, Microelectronic Circuits. The Claim 15 reciting the limitations of Claim 11, rejected accordingly, additionally requires replacement of NPN transistors by PNP transistors. A. Sedra and K. Smith textbook discloses. A. Sedra and K. Smith textbook discloses (Fig. 8.9 and 8.10, pp. 408 – 410) that NPN and PNP transistors are functionally equivalent and differ only in their polarity. As seen in Fig. 8.10 the same functionality can be obtained by replacing NPN transistor (Fig. 8.10a) by PNP transistor connected in a mirror reversed manner (Fig. 8.10b). Accordingly, the PNP emitter plays a role of the NPN collector and PNP collector plays a role of the NPN emitter. Both transistors of Avery circuit (Qs and Ql in Fig. 7 of Avery) are subject to this conversion. The resistors remain positioned according to Avery

(element Rs in Fig. 7), i.e. between the bases of transistors and the power source terminal (element 20 in Fig. 7 of Avery). The circuit obtained in such transformation is a full equivalent of the original Avery circuit and satisfies all the limitations of Claim 14.

Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 5,272,371, US 5,821,797, US 5,539,327.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
06/03/2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800